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Terms	Documents
(bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3)	14

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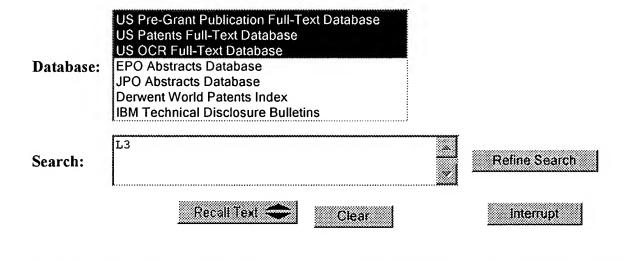
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DB=PC	GPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L1</u>	(bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3)	59	<u>L1</u>

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Terms	Documents
(370/461 370/462 710/110 710/113 710/40 710/107 710/305 710/244 710/36 710/58 710/112 710/48 711/147 711/100 340/825.5 340/825.51).ccls.	9646



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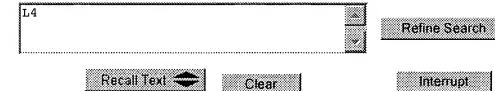
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L1 and L3	37

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<u>L3</u>	710/110,113,40,107,305,244,36,40,58,112,48;370/461,462;340/825.5,825.51;711/147,100.ccls.	9646	<u>L3</u>
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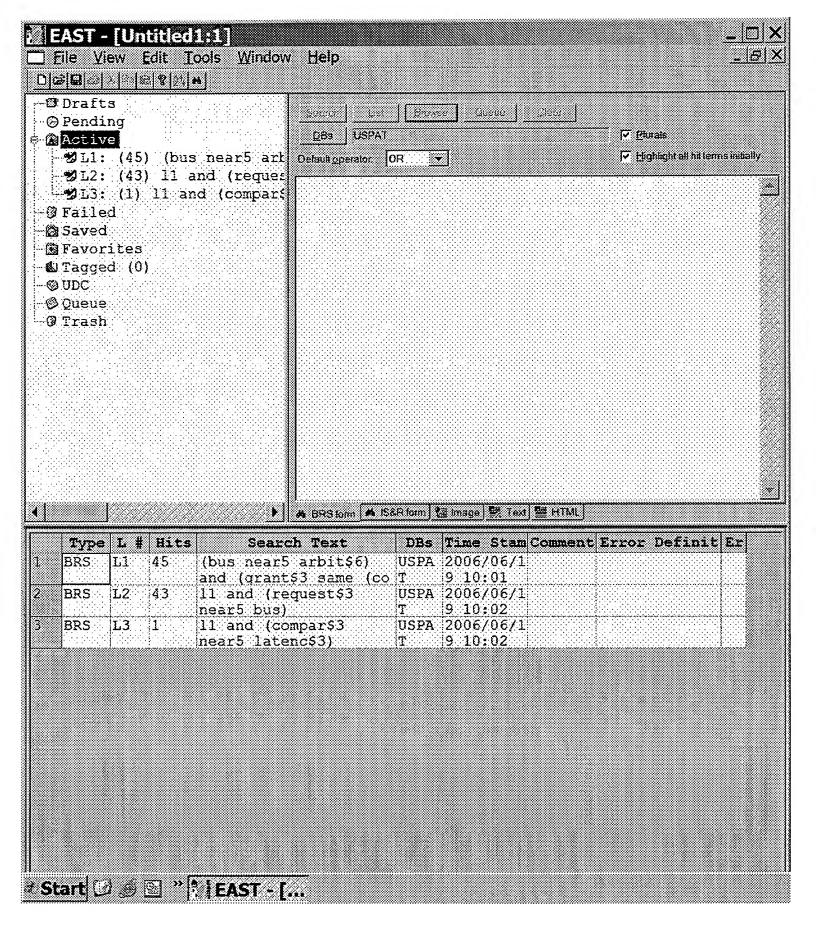
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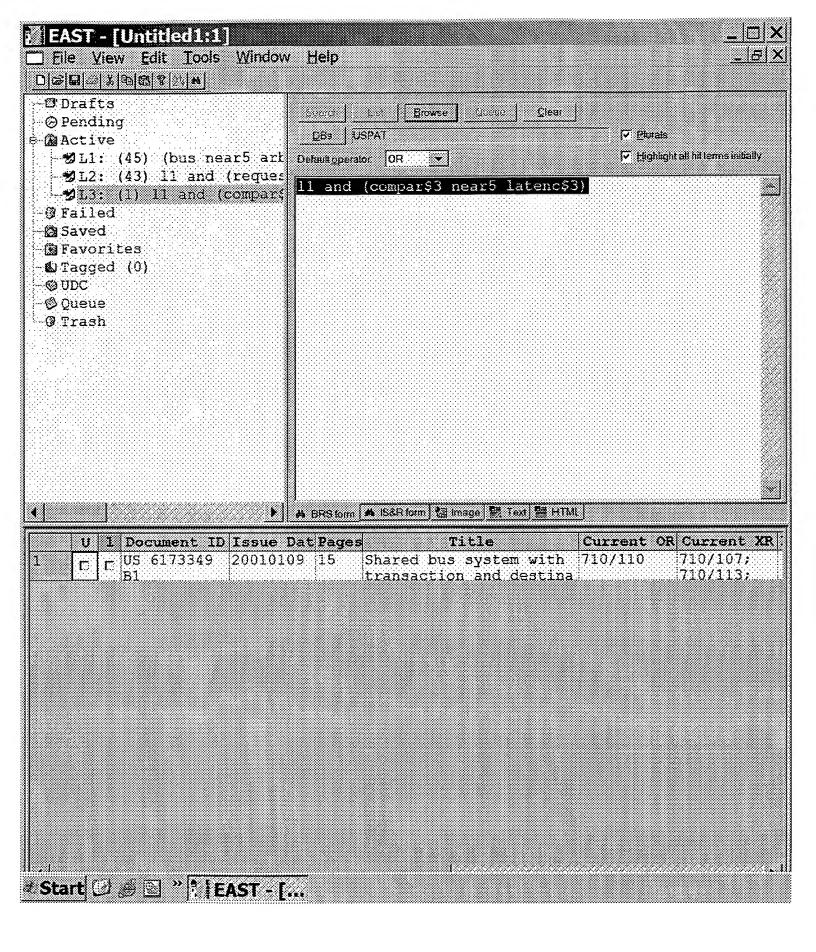
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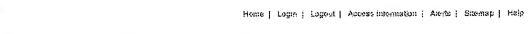
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Performance model for a prioritized multiple-bus multiprocessor system

Kurian, L.; Yu-Cheng Liu; Parallel and Distributed Processing, 1994. Proceedings, Sixth IEEE Symposium on 26-29 Oct. 1994 Page(s):577 - 584 Digital Object Identifier 10.1109/SPDP.1994.346120 AbstractPlus | Full Text: PDF(488 KB) INSEE CNF Rights and Permissions 7. A fluid flow tracking arbiter for input buffered ATM switch with heterogeneous port bandwidth Global Telecommunications Conference, 2003. GLOBECOM '03. IEEE Volume 6, 1-5 Dec. 2003 Page(s):3138 - 3143 vol.6 Digital Object Identifier 10.1109/GLOCOM.2003.1258814 AbstractPlus | Full Text: PDF(256 KB) KEILE CNF Rights and Permissions 8. The multiprocessor system with a fairly weighted global bus arbitration circuit Deshmukh, R.G.: Doi, S.: Southeastcon '90. Proceedings. IEEE 1-4 April 1990 Page(s):750 - 754 vol.2 Digital Object Identifier 10.1109/SECON.1990.117917 AbstractPlus | Full Text: PDE(300 KB) IEEE CNF Rights and Permissions 9. Point-to-point connectivity between neuromorphic chips using address events Boahen, K.A.: Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] Volume 47, Issue 5, May 2000 Page(s):416 - 434 Digital Object Identifier 10.1109/82.842110 AbstractPlus | References | Full Text: PDF(888 KB) | IEEE JNL Rights and Permissions 10. Architecture and performance comparison of a statistic-based lottery arbiter for shared bus on chip Yan Zhang; Design Automation Conference, 2005, Proceedings of the ASP-DAC 2005, Asia and South Pacific Volume 2, 18-21 Jan. 2005 Page(s):1313 - 1316 Vol. 2 Digital Object Identifier 10.1109/ASPDAC.2005.1466585 AbstractPlus | Full Text: PDF(194 KB) IEEE CNF Rights and Permissions 11. A generic programmable arbiter with default master grant Petrot, F.: Hommais, D.: Circuits and Systems, 2000, Proceedings, ISCAS 2000 Geneva. The 2000 IEEE International Symposium on Volume 5, 28-31 May 2000 Page(s):749 - 752 vol.5 Digital Object Identifier 10.1109/ISCAS.2000.857610 AbstractPlus | Full Text: PDF(300 KB) IEEE CNF Rights and Permissions 12. Some solutions for FIP network interconnection Saba, G.; Mammeri, Z.; Thomesse, J.P.; Factory Communication Systems, 1995. WFCS '95, Proceedings, 1995 IEEE International Workshop on 4-6 Oct. 1995 Page(s):13 - 20 Digital Object Identifier 10.1109/WFCS.1995.482645 AbstractPlus | Full Text: PDF(620 KB) IEEE CNF Rights and Permissions 13. Ordered arbiters Bystrov, A.; Yakovlev, A.; **Electronics Letters** Volume 35, Issue 11, 27 May 1999 Page(s):877 - 879 AbstractPlus | Full Text: PDF(328 KB) IEE JNL



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Ordered arbiters

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Publication Date: 27 May 1999 Volume: 35 , Issue: 11 On page(s): 877 - 879

INSPEC Accession Number:6278050 Posted online: 2003-07-09 09:39:02.0

Abstract

ISSN: 0013-5194

The granting of requests in the order of their arrival is not satisfied in existing I/n arbiters, such as token rings, tree arbiters and networks of two-way arbiters. The proposed solution stores pending grants in a FIFO, thus maximally preserving the request order, improves fairness and offers lower metastability rate.

Index Terms

Inspec

Controlled Indexing

network interfaces

Non-controlled Indexing

FIFO storage asynchronous systems metastability rate reduction ordered arbiters pending grants storage request order preservation

Author Keywords

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